High Performance in a Small Form Factor

Embedded Tech Trends

January 21-22, 2013

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ADLINK Technology

Agenda

❖ **Basics of SWaP (and more)**

❖ **SWaP Economics**

❖ **ADLINK Overview**

❖ **Improving Efficiencies**

❖ **SFF System**

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Basics of SWaP

Elements of "SWaP²C²R"

- Demand for Performance & Reliability drives demand for better Cooling

- Constant pressure to decrease Size, Weight, Power, and Cost

Size   Performance   Weight   Reliability   Power   Cooling   Cost

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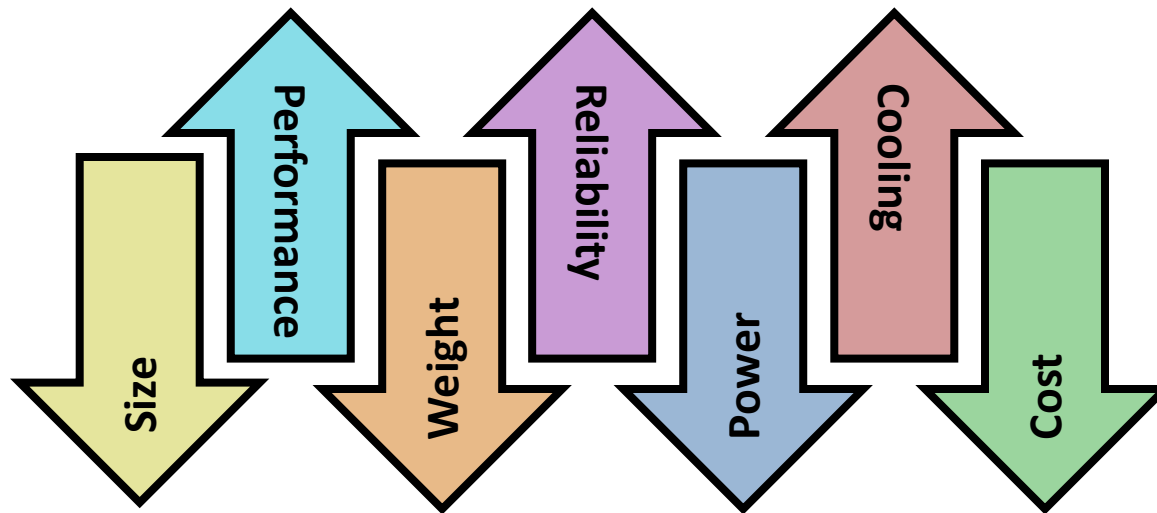
SWaP Economics

Size (Form Factor)

- Size reduction is #1 Goal

    - **Drives weight reduction**

    - **Drives cost reduction**
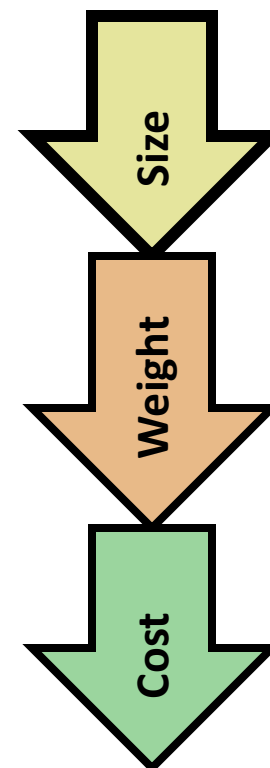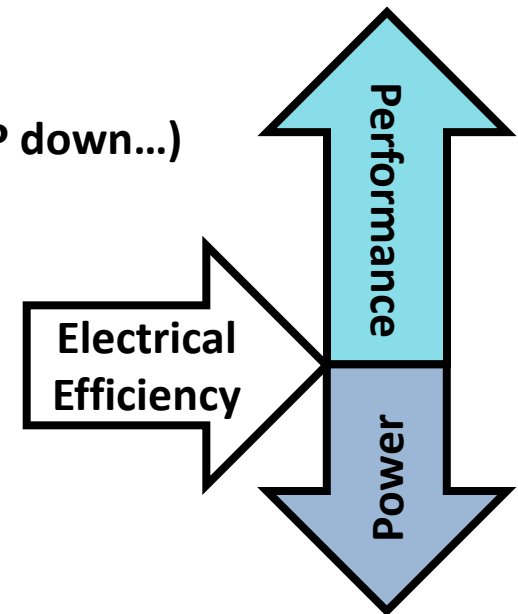
6U VPX → **3U VPX** → **VITA-75**
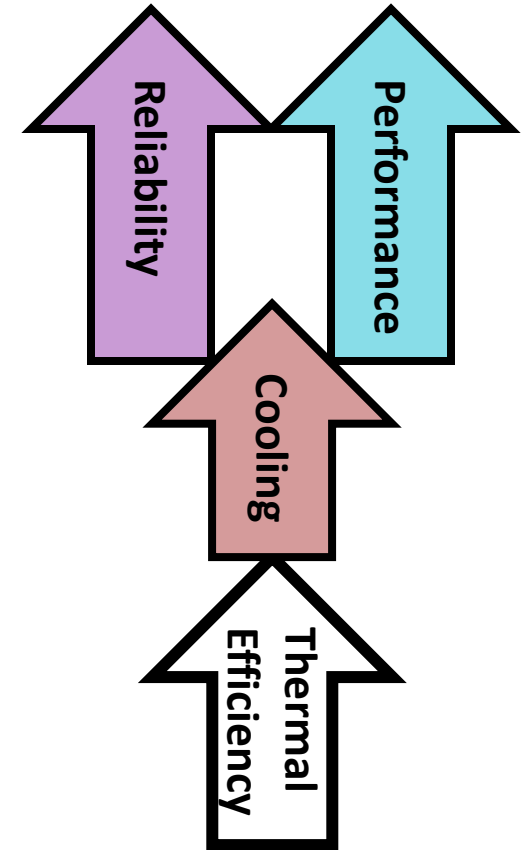
SWaP Economics

Power & Performance

▪ Modern applications hungry for performance

- **Multi-Sensor Data Capture**

- **Processing Threat Assessment**

▪ High efficiency hardware and increase performance

- **Advanced power management features (IFFS, TDP down...)**

- **Smaller process 22nm -> 14nm ->**

- **Lower voltages**

Performance

Electrical Efficiency

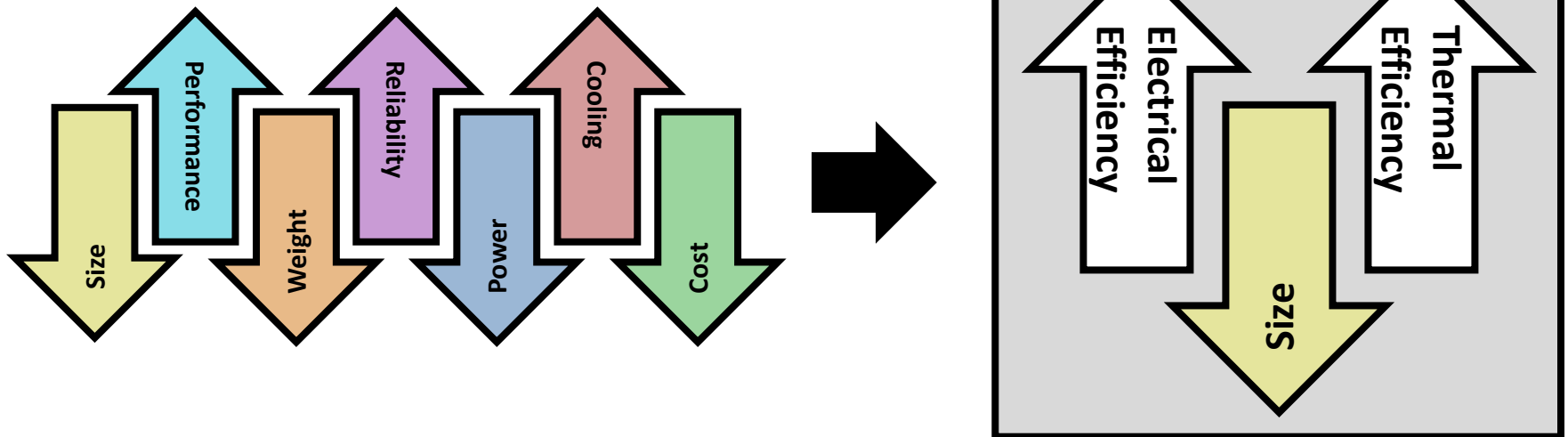**Power**

SWaP Economics

Cooling

- Increased cooling improves performance

- Increased cooling improves reliability

- Better cooling comes from higher thermal efficiency

SWaP Economics

SWaP²C²R Design Keys

- Size reduction

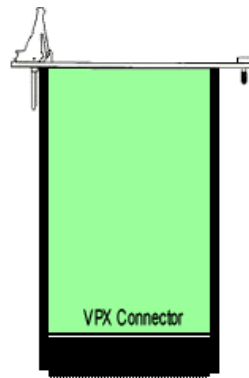- Thermal efficiency
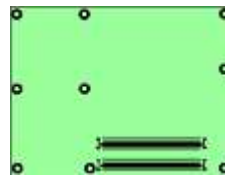
- Electrical efficiency

ADLINK Overview

Form Factors

- Produces COM Express, PC/104, VPX, and others

- Formed PC/104 Consortium in 1992

- Invented PC/104 *Plus* in 1996

- Introduced Small Form Factor Systems based on EBX SBCs in 2008

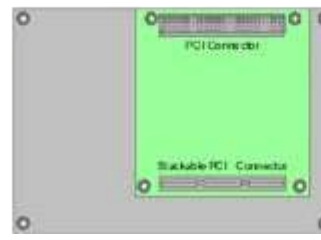- Ratified PCI/104 Express in 2011, capable of 448 GT/s (55GB/s)
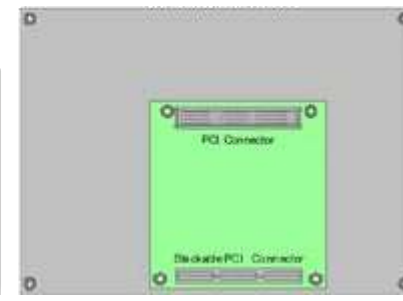
VPX 3000™
(VPX 3U™ Form Factor)

COM Express Tye2/6
(Basic/Compact/Mini
Form Factors)

Core Module™
(104™ Form Factor)
90 x 96 mm

ReadyBoard™
(EPIC™ Form Factor)
115 x 165 mm

LittleBoard™
(EBX™ Form Factor)
146 x 203 mm

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Improving Efficiencies

Thermal Efficiency
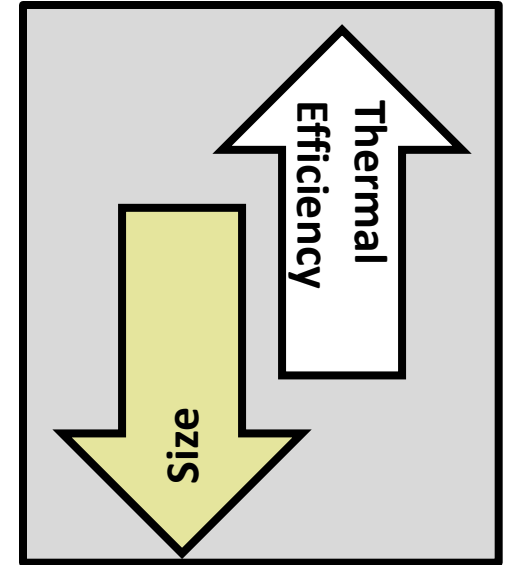
- Shorten thermal pathways

- Limit thermal interfaces

Size Reduction

- Eliminate Backplanes

- Eliminate COM Carrier

- Eliminate IO Carriers

- Miniature high density SMT connectors (required as IO signaling speed increases)

Also reduces size

Also increases reliability

Thermal Efficiency

Size

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Improving Efficiencies

Internal Size Reduction

- Backplane & Carrier Elimination

- Smaller Expansion IO Form Factor

- Smaller Bus connectors
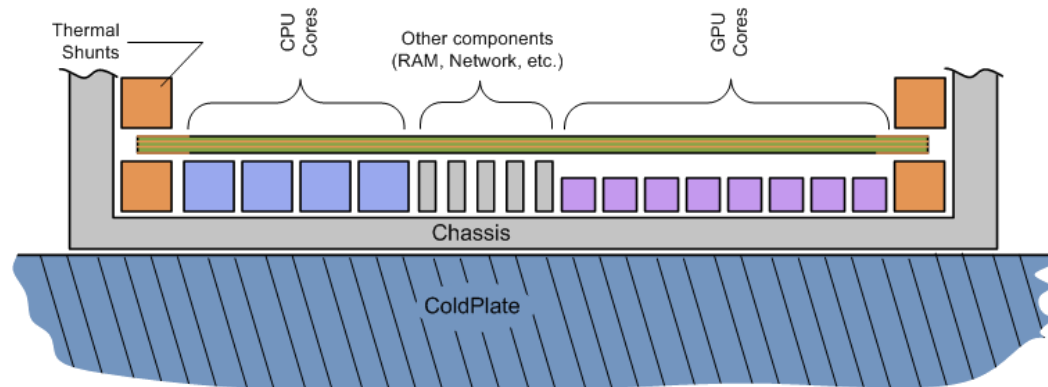

Thermal Efficiency ↑

Size ↓

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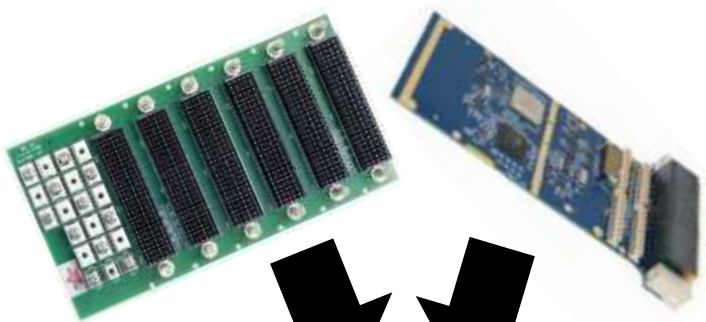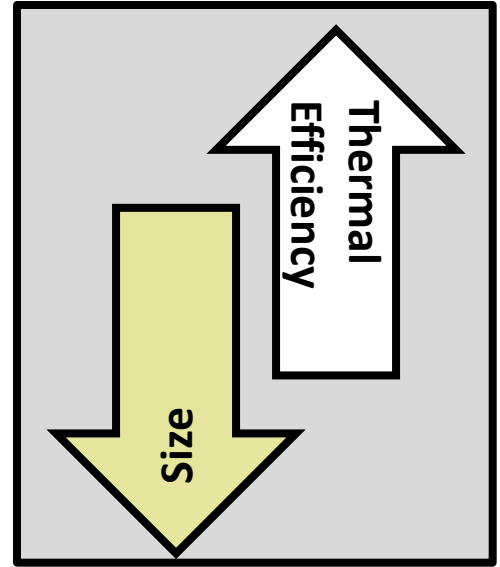
Improving Efficiencies

Cardcage Thermals

▪Long thermal pathways

▪Multiple interfaces

▪Large ΔT (Die-Coldplate)

▪Low Heat Flux Density at Coldplate

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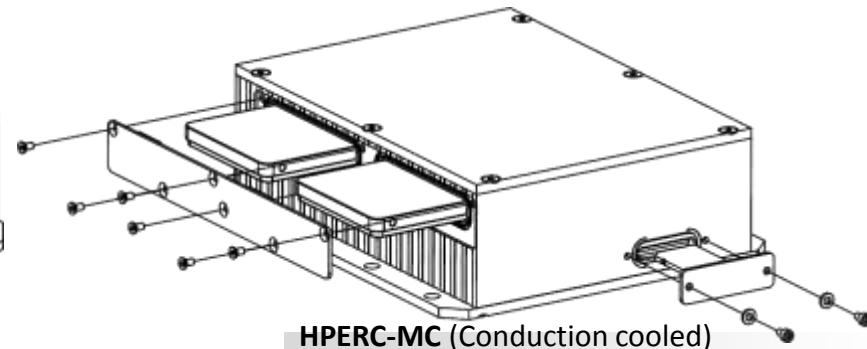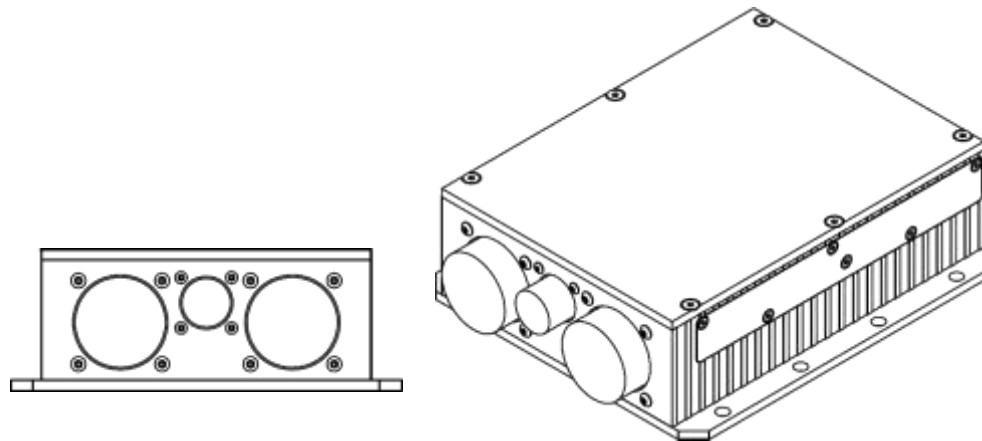TECHNOLOGY INC.
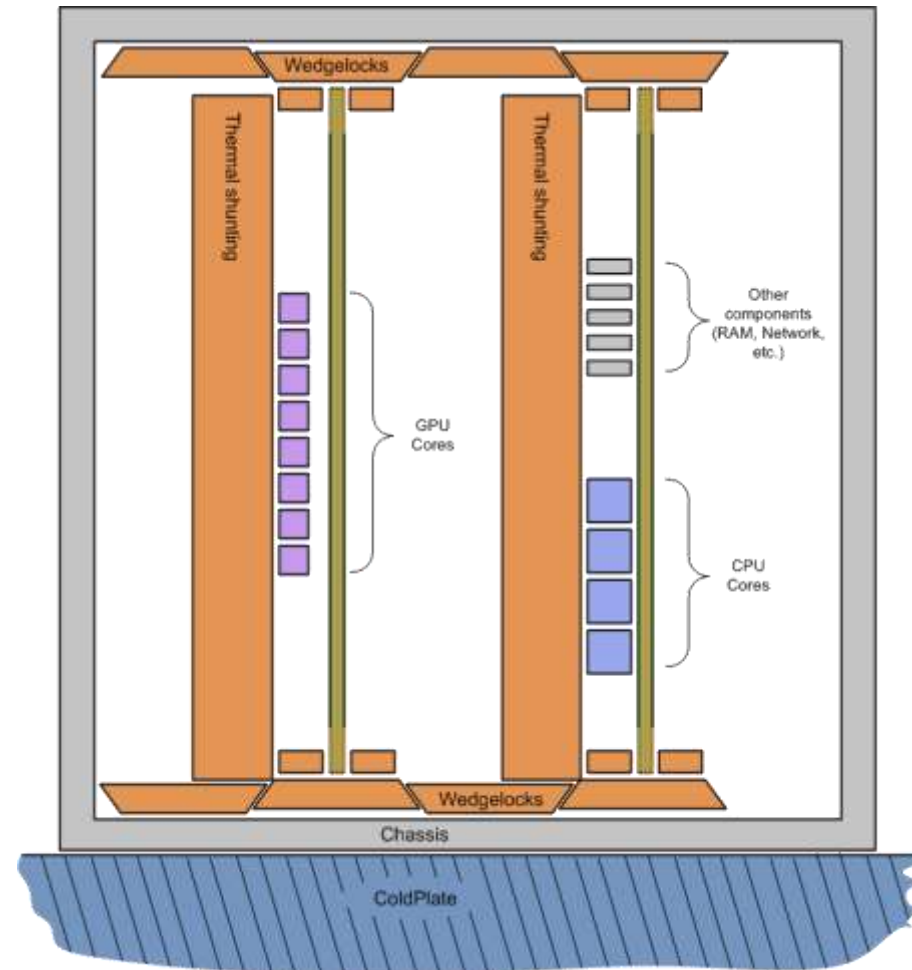
Improving Efficiencies

SFF Thermals

▪Direct chassis connection

▪Single interface

▪Short pathway

▪Smaller ΔT (Die-Coldplate)

▪High heat flux density at coldplate

▪More Efficient Dissipation

▪Decreased contact area

Thermal Shunts | CPU Cores | Other components (RAM, Network, etc.) | GPU Cores

Chassis

ColdPlate

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SFF System

VITA-75 Application Ready Platform

▪Small Standard Form Factor (63.5 x 150 x 203.4mm,
2.0 Kg) **INCLUDES dual 2.5" SSD RAID, GP-GPU, PCI/104 Express, and mPCIe card installed**

▪VITA-75.20/21/22 compliant mounting

▪High Performance / Power Efficient

- Intel™ Gen3 Quad Core® i7
- Nvidia or AMD GP-GPU

HPERC-M (Free air convection)

HPERC-MC (Conduction cooled)

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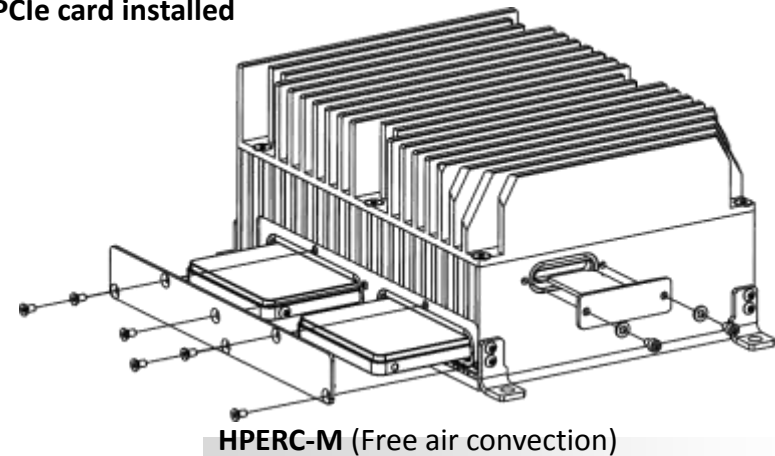
High Performance in a Small Form Factor

Embedded Tech Trends

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